## REMARKS

**[1-2]** Claims 1-5 are canceled without prejudice to reentry.

**[3]** Claim 7 is amended as the Examiner suggested and in keeping with how it has already been examined (¶3 on page 2). Claims 10-13 were amended as the Examiner suggested to correct misspelling. The specification is amended accordingly. The title is also amended.

**[4]** Claims 6-8, 10-11, and 13 were rejected under §102 over Kinzer '067. This rejection is moot as to claim 6, which now has the same subject matter as canceled claim 9; the rejection of claim 6 is discussed below, as is the rejection of claims 8 and 10 depending from claim 6.

**Claim 7.** Claim 7 recites *wherein the width of the cell is smaller than 2μm.* The Examiner points to Fig. 2 of Kinzer as anticipating this feature. However, no dimensions are shown in Fig. 2 and there is no other citation. No disclosure of the cell width is seen in Kinzer, either in the discussion of Fig. 2 or in that of applied Fig. 8. With respect, there is no support for the Examiner's assertion.

Furthermore, the region 202 which the Examiner applies is not a *low resistance region forming a part of an inner wall of a hole,* because it is found only at the <u>bottom</u> of the asserted hole.

**Claims 11 and 13.** These claims are allowable for depending from an allowable base claim.

**[5-7]** Claims 9 and 12 were rejected under §103 over Kinzer '067 in view of Darwish '520. This rejection is respectfully traversed.

**Claim 6.** Claim 6, as exemplified in Fig. 1, recites

6. *A semiconductor device comprising:*

*a plurality of cells each including a drain region* [2] *of a first conductivity type* [N−], *a channel region* [5] *of a second conductivity type* [P−] *different from the first conductivity type and a source region* [6] *of the first conductivity type* [N+] *stacked in this order on a semiconductor substrate* [1] *so as to be capable of forming a channel in a direction of a thickness of the semiconductor substrate; and*

*a low resistance region* [10] *of the second conductivity type* [P+] *having a conductivity higher than that of the channel region* [P−], *the low resistance region forming a part of an inner wall of a hole formed between adjacent ones of the plurality of cells, the low resistance region extending in an isotropic manner with respect to a predetermined region in the hole so as to be in contact with the channel region* [5],

*wherein the drain region* [2] *is shared by the plurality of the cells; and*

*wherein the low resistance region* [10] *and the drain region* [2] *are in contact with each other.*

The low resistance region 10 provides a low base resistance Rb for the parasitic transistor T, as shown by a schematic symbols in Fig. 1, and therefore helps to avoid avalanche breakdown (page 21, line 22 to page 22, line 24).

**The Delta Layer Has the Wrong Doping.** The Examiner states that the claimed low resistance region is not disclosed by Kinzer, and relies on Darwish for this feature, citing "delta layer" 402 of Darwish. The Applicant respectfully disagrees because the delta layer 402 has N-type doping, which is the *same* type as that of the adjacent drift (drain) region 111 (col. 2, lines 7-9 and col. 5, lines 41-42).

In contrast to Darwish, the Applicant's exemplary Fig. 1 shows that the low resistance region 10 is doped P+ while the drain region 2 is oppositely doped N−, and claim 6 itself recites *a drain region* [2] *of a first conductivity type* [and] ... *a low resistance region* [10] *of the second conductivity type*. Thus, there is no anticipation of the claimed feature.

**Contact With the Drain.** The Examiner identifies the low resistance regions of the two references as 202 (Kinzer) and 402 (Darwish). However, with respect, region 202 of Kinzer best corresponds to region 114/116 of Darwish, rather than to region 402. Region 114/116 is: doped P+, as is region 202; in contact with the upper electrode (102 Kinzer, 118 Darwish); and in contact with the N+ source regions (109, 112); in all these, similar to region 202. The Applicant sees that 402 has no corresponding part in Kinzer.

Kinzer's P+ region 202 is not in contact with the drain, contrary to amended claim 6. Darwish's P+ body 114/116 is in contact with the drain, but this body 114/116 is not a "low resistance region"—it is the channel itself, corresponding to channel 100 of Kinzer. Because body 114/116 *is* the channel region, it cannot be *in contact with the channel region* as claim 6 recites, and it cannot have *a conductivity higher than that of the channel region* as claim 6 recites.

Because regions 202 and 402 do not correspond, it is respectfully submitted that it would not have been obvious to increase the depth of the P+ region, as the Examiner asserts at the bottom of page 4.

The true low resistance region of Darwish is 402, and Darwish discloses it to be such (see below). With respect, however, region 402 is not *part of an inner wall of a hole ... extending in an isotropic manner with respect to a predetermined region in the hole so as to be in contact with the channel region* and therefore does not meet the Applicant's claim language.

**Darwish Teaches Against Adding the Delta Layer to Kinzer.** Darwish shows as its prior art Figs. 1 and 2A a structure like Kinzer's applied Fig. 8, and Figs. 3A-3C show prior art with the deep central P+ region.

Darwish states (col. 3, lines 30-44), "The deep central P+ region 114 [of Fig. 3], while greatly reducing the adverse consequences of breakdown, also has some unfavorable effects ... the presence of a deep P+ region 114 tends to pinch the electron current as it leaves the channel and enter the drift region 111. *In an embodiment which does not include a deep P+ region* [such as Kinzer], *the electron current spreads out* when it reaches the drift region 111. .... The presence of a deep P+ region limits this current spreading and increases the on-resistance" (emphasis added).

Darwish's solution to the current pinch caused by the deep P+ region is that "The trench MOSFET of this invention includes ... a 'drift' region [111] ... [and] To promote current spreading at the lower (drain) end of the channel region when the MOSFET is turned on, a 'delta layer' is provided within the drift region" (col. 3, line 52 to col. 4, line 2).

Thus, Darwish teaches that no delta layer is needed unless there is a deep P+ region. Kinzer lacks that type of region. Therefore, Darwish teaches that Kinzer needs no delta layer.

**The Proposed Motivation.** With respect, the motivation for combing references proposed by the Examiner is incorrect. If Kinzer's region 202 were made deep, as the Examiner proposes at the bottom of page 2, then the resistance would be not lowered but instead would be raised, according to the teaching of Darwish (discussed above).

**Claims 10 and 12.** These claim are patentable for depending from claim 6. Furthermore, these claims recite, *wherein the low resistance region and the source region (or, source driving electrode) are in contact with each other*. This feature is shown in Fig. 8 of Kinzer. However, if Kinzer were modified according to Darwish as the Examiner asserts, then the contact would be

lost because the low resistance region would move down into the drain. This teaches against combining the references to reach claims 10 and 12.

**Inner Wall of a Hole.** The claimed *low resistance region forming a part of an inner wall of a hole* is not seen in the references. Kinzer's hole extends only into the source region and does not meet the claim, as noted above in regard to claim 7. Darwish has no hole whatsoever. No combination of the references (not admitted obvious) could reach claim 6.

**Claim 15.** New claim 15 recites that the hole extends into the drain region. Neither reference shows any hole extending into the drain region.

For the reasons above, withdrawal of the rejection is requested.

Respectfully submitted,

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*I certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office (fax no. 571-273-8300) on May 5, 2006.*

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